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Design specification and simulations of a Miller compensated Operational Amplifier with 75dB Gain

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Abstract

This paper presents a two-stage Miller compensated operational amplifier design using cadence 55nm CMOS technology. This circuit provides a single ended output due to mirror pole is implemented while the input of this operational amplifier is differential. A biasing circuit is also designed and attached with this amplifier. This operational amplifier provides a gain of 75.41dB while the phase margin is off 70°. The Gain bandwidth of this operational amplifier is 9.5MHz. The power consumption of this overall circuit including the biasing circuit is 154.69µW. The other performance parameters are also analyzed and provide in this paper. The mathematical calculation for the circuits is also presented. Due to medium power consumption and higher gain bandwidth this amplifier can be used in different data converters like Delta-Sigma ADC. Because the performance of this ADC is depending upon the higher Gain Bandwidth.

Keywords: Gain bandwidth; Miller compensated; Mirror pole; Operational Amplifier; Slew-rate.

1. Introduction

An amplifier is an important building block for Data converters. The performance of the Delta sigma ADC depends upon the specifications of the operational amplifier. The Gain bandwidth, the open loop Gain of operational amplifier, phase margin and slew rate are the performance parameters of the operational amplifier. In this paper [3] a miller compensated two stage operational amplifier is designed using TSMC 0.18µm CMOS technology. This amplifier is designed to attain the requirements of delta sigma analog to digital converters like high resolution and high speed. But the disadvantage of this design is the power consumption which is 16.5mW. So, this design is not so good for low power applications. In another design [4] a miller compensated two stage operational amplifier is designed to meet the specifications. This design consists of an NMOS amplifier along with active load as first stage which is followed by PMOS amplifier

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at second stage which attain a pole splitting and hence the operational amplifier compensation. This design is also a single ended output design, and the biasing circuit is attached. The power consumption of this operational amplifier is also greater which is not so good for data converter applications. A critical review of two stage miller compensation operational amplifier is proposed in this paper [5]. The trade of is also considered which is involved in small signal parameters and compensation capacitor value, as the second stage need a more biasing current it is working with a large load capacitor to attain phase margin. A method is presented to increase the transconductance without increasing the power consumption at second stage. A 65nm CMOS technology is used to perform the simulations with supply voltage of 1 volt.

Circuit Diagram:

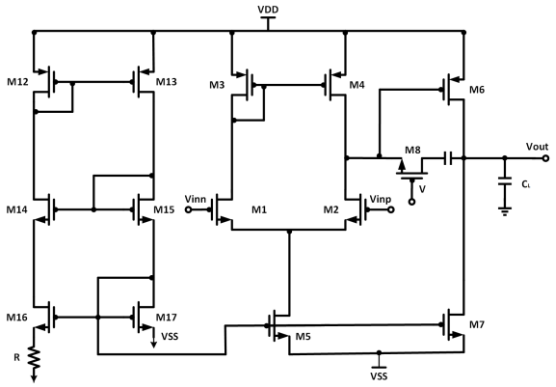

Figure 1: Schematic diagram of Op-Amp with biasing circuit

A miller compensated two stage operational amplifier is shown in the figure1. This circuit include a two-stage operational amplifier and stable transconductance biasing circuit. The gain which is attain from 1st stage is usually high while due to common source technique the gain at second stage is moderate. As there is biasing circuit include so there is no need to provide biasing from other source. The input of the operational amplifier is differential while the output is single ended. The transistor M8 in the circuit is used as a resistor and we provide supply voltage to its input.

Design Calculations:

In this section we will determine the equations for the calculations of aspect ratios of transistor using the basic operational amplifier equations.
From MOSFET, strong inversion, square law equations:
According to this equation drain current (I_D)

$$I_D = \frac{1}{2}\beta V_{ov}^2$$

Where the value of β is dependent upon the oxide capacitance and aspect ratio of the transistor.

$$\beta = \mu_n C_{ox}\left(\frac{W}{L}\right)$$

The transconductance of the amplifier is

$$g_m = \frac{2*ID}{Vov}$$

For NMOS $V_{ov} = (V_{gs} - V_{tn})$ and for PMOS $V_{ov} = (V_{SG} - |V_{tp}|)$

Compensation capacitor is design in such a way that pole P_2 is 2.2 time more than the GBW which will provide a 60^0 of phase margin. Now the next phase is to design the estimated biasing current. As we know

Slew rate (SR) = I_{ss}/C_c.

Where Iss= I_5 which is the tail current. By using this equation, we can find tail current.

Now we assume that gain bandwidth is established by dominant node, so

G_{m1} = GBW * C_c

And

$(W/L)_{1,2}$ =$(gm_1)^2/k_n*I_5$

From here we can find the aspect ratio of the transistor 1 and 2

For the aspect ratio of transistor 3 and 4

$$(W/L)_{3,4}= \frac{I5}{kp*[Vdd-Vin(max)-|Vtp,3|(max)+Vtn,1(min)]2}$$

Design for aspect ratio of transistor 5 from minimum input voltage.

$V_{DS5} = V_{in}(min) - Vss - \sqrt{\frac{I_1}{\beta_1}} - V_{tn,1}(max)$

After calculating this we can find the aspect ratio is it depends upon the value of V_{DS5}.Now

$$(\frac{w}{l})_5 = \frac{2I_5}{k_nC_{ox}*(V_{DS5})2}$$

Now finally the aspect ratio of 6 transistor can be calculated by finding the transconductance of transistor 4 and 6.

$g_{m6} = 10* g_{m1}$

Now

$$(\frac{w}{l})_6 = (\frac{w}{l})_4 * \frac{g_{m6}}{g_{m4}}$$

$$(\frac{w}{l})_7 = (\frac{w}{l})_5 * \frac{I_6}{I_5}$$

$$(\frac{w}{l})_8 = \frac{(\frac{w}{l})6}{1+\frac{C_l}{C_c}}$$

By putting the values of our specifications, we can calculate the aspect ratios of all transistors from these above equations. And then put these values in circuit and then we have to optimize these ratios.

Design Equations of bias Circuits:

Current mirror M12,M13 causes M17 to conduct a current equal to that in M16. i.e I_B .

$$I_B=\frac{1}{2}\mu_nC_{ox}(\frac{W}{L})_{16,17}(V_{GS16,17}-V_T)^2$$

Applying K.V.L on V_{GS} of M_{16} and M_{17}

$$-V_{GS17}+V_{GS16}+I_BR_B=0$$

$$V_{GS17}=V_{GS16}+I_BR_B$$

Subtracting Vt from both sides

$$(V_{GS17}-Vt) =(V_{GS16}-Vt) +I_BR_B$$

$$I_B = \frac{2}{\mu_nCox\left(\frac{W}{L}\right)_{16}{R_B}^2}\left(\sqrt{\frac{\left(\frac{W}{L}\right)_{16}}{\left(\frac{W}{L}\right)_{17}}}-1\right)^2$$

$$I_B \propto \frac{1}{{R_B}^2}$$

$$R_B=\frac{2}{g_{m16}}\left(\sqrt{\frac{\left(\frac{W}{L}\right)_{16}}{\left(\frac{W}{L}\right)_{17}}}-1\right)$$

Here, $g_{m16}=\sqrt{\mu_nCox\left(\frac{W}{L}\right)_{16}I_B}$

In order to generate 18µ of biasing current we use 0.52KΩ resistance.

Simulation

A miller compensated two stage operational amplifier is designed in 55nm CMOS technology. The first stage of the amplifier gives the high gain while the second stage provide moderate gain. The biasing circuit is also designed and attached to the operational amplifier instead of providing the DC voltage source. The Op-Amp has differential input and single ended output. The Load capacitance of capacitor is 100fF.

C_c= 200fF and C_L=100fF

After performing the simulations, we attain a performance parameters like gain and phase of Op-Amp which is 75.41dB and 70^o respectively. The plot of the gain and phase shown in the figure 2.

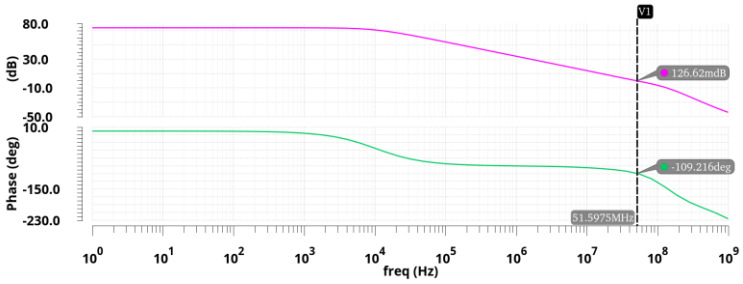

Figure 2: Gain and Phase plot

The offset voltage of this operational amplifier is <1mV which is attain from DC transfer curve. The open loop DC gain of the operational amplifier is 4870V/V. we also can calculate the input offset voltage by the formula given below.

Input offset voltage = $\frac{output\ offset\ voltage}{Open\ loop\ DC\ gain}$

The unity gain frequency of this circuit is 51.6MHz while the gain Bandwidth product is 9.5MHz.

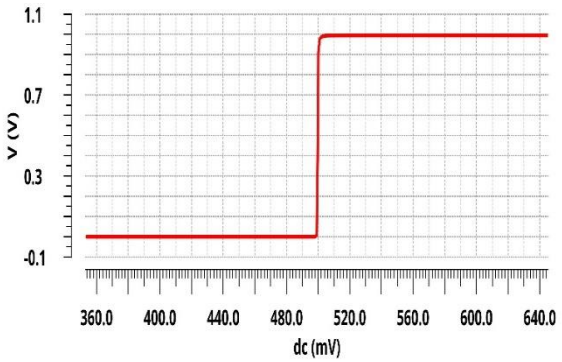

Figure 3: DC transfer curve

The step response of this operational amplifier is shown in the figure 4. We can find the slew rate of the operational amplifier from this plot whose value is 33 V/µs. All the performance calculations are shown in the table below.

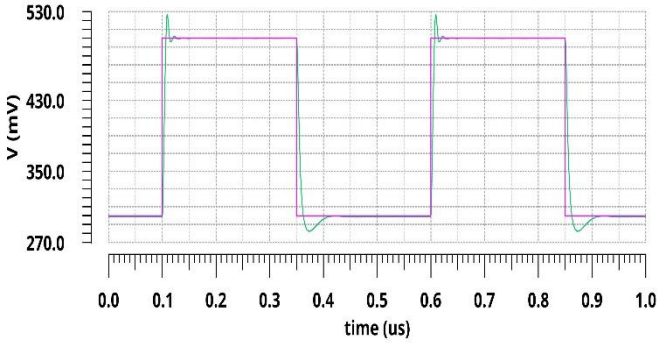

Figure 4: step response of Op-Amp

Table 1: Performance

Parameters	Values
Open loop gain	75.41dB
Phase margin	70^{o}
Gain bandwidth	9.5MHz
Output offset voltage	<1mV
Unity Gain Frequency	51.6MHz
DC gain	4870 V/V
Slew Rate	33 V/µs
Power consumption	154.69µW

2. Conclusion

A two-stage miller compensation operational amplifier is designed in cadence 55nm CMOS technology for different types of data converters. The schematic diagram of the circuit is presented in the figure. The operational amplifier attains a gain of 75.41dB with the phase margin of 70^{o}. The gain bandwidth of the operational amplifier is 9.5MHz while the other performance parameters are also calculated. The power consumption of the operational amplifier is 154.69µW while the supply voltage of 1 Volt.

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