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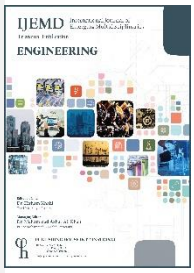

Design of a 92 dB Fully-Integrated Low Voltage Folded Cascode OTA with Class AB Output Buffer and gain-enhancement in 55 nm CMOS Technology

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Abstract

This paper presents a design of folded cascode operational transconductance (OTA) amplifier with class AB output buffer and a gain-enhancement circuit. The proposed circuit is suitable for low-voltage operation in applications with limited power and high gain bandwidth product (GBW). All MOSFETs in the proposed architecture conduct 12 µA of current under equilibrium conditions. The speed of the op-amp is increased by a fully-integrated biased circuit that is designed to boost the currents and overdrive voltages of the MOSFETs. By adjusting the drain of the cascode current sources to increase the output resistance, a class AB output buffer is placed at the folded cascode OTA's output node. Differential amplifier circuits with source-follower level shifters are added to the folded-cascode architecture for gain-enhancement. This scheme enhances the gain which is necessary for precision amplification. The overall circuit simulation results using industry-standard CMOS 55-nm technology reveal improved performance as compared to state of the art. The proposed folded cascode OTA with class AB output buffer and gain-enhancement scheme operates on a supply of 1 V and offers a DC gain of 92 dB, phase margin of 66^0 and a gain bandwidth (GBW) of 3 MHz.

Keywords: Gain bandwidth; OTA; Output buffer; Phase margin; Transconductance.

1. Introduction

An essential component of analog and mixed signal circuits is the operational amplifier. The DC gain of amplifiers is rapidly declining as transistor dimensions are gradually reduced. Thus, applications that require high gain amplifiers provide serious design challenges. Amplifiers with DC gains in the order of 90 to 100 dB are usually needed in applications such as switched capacitor circuits, data converters, and other high gain applications. Even with two stage architectures, deep sub-micron devices make it difficult

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to attain such a magnitude of gain. The DC gain must then be increased using alternative techniques, such as gain-enhancement. A common-source output buffer (an op-amp) with two diff-amps with source-follower level shifters [1] added to PMOS and NMOS networks respectively, act as a gain booster while keeping the overdrive voltage constant.

Gain boosting techniques [1–3] increase gain significantly by increasing the output resistance of the amplifier. Three amplifiers operating at different common mode levels are typically used in a fully differential gain boosted folded cascode amplifier. Traditional methods for designing such cascode amplifiers are time-consuming and have been presented in previous works [4-8]. Many designers use an ad hoc mechanism, adjusting device dimensions, and attempting to bring all transistors into saturation in order to meet the target specifications. The disparity between analytical expectations and simulation results is primarily due to short channel device modeling using long channel equations.

In this work, a design of fully-integrated low voltage folded-cascode OTA using additional circuits that act as gain booster i.e., class AB output buffer with gain-enhancement amplifier circuits, is presented. Assuming the same biasing conditions, device sizes, and overdrive voltages in the basic topology of folded cascode OTA [9], the proposed op-amp circuit offers better input common-mode voltage range and output swing as well as improved high-speed operation.

A brief explanation of the class AB output buffer is provided in the following section, which is followed by the design of a fully-integrated folded cascode operational transconductance amplifier.

Class AB Output Buffer Circuit

The Class AB amplifier output stage combines the advantages of the Class A and Class B amplifiers while minimizing the problems of low efficiency and distortion associated with them, resulting in a better amplifier design. The typical circuit of CMOS based class AB output buffer is shown in Figure 1. The detailed elaboration of the buffer circuit can be found in [10,11].

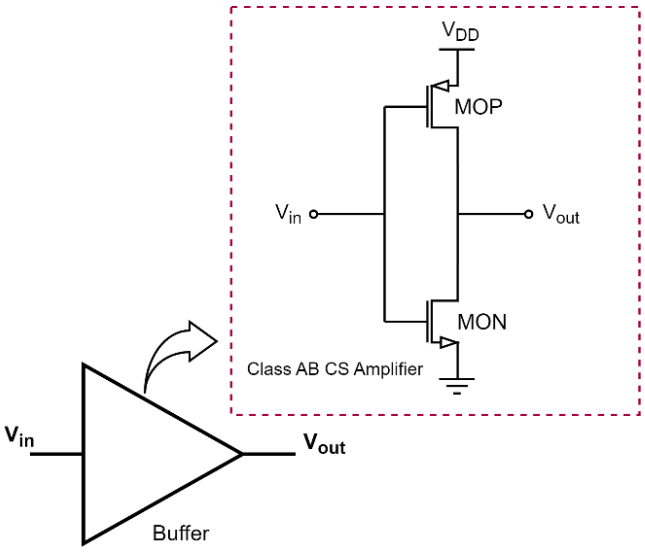

Figure 1: Output Buffer circuit

The output buffer is mostly used to drive large capacitive and resistive loads therefore the gain of the second stage of folded cascode OTA drops but, since the gain of first stage is quite large, the op-amp ends up with a reasonably high overall gain. The detailed discussion is provided in the proceeding section.

Structure of the Proposed Folded Cascode OTA

NMOS Input transistor

The operational amplifier's gain is provided by the input stage. Because NMOS devices have greater mobility, PMOS input differential pairs have lower transconductance than carrier NMOS pairs. As a result, the NMOS transistor is chosen to provide the highest gain possible.

Architectural Evaluation

The operational amplifier serves as the primary bottleneck in an analog circuit. The designer has access to a variety of OTA configurations that tend to enhance performance requirements. Because of the "folded cascode" op-amp's high gain and bandwidth capabilities, we choose it. Figure 2 represents the proposed folded cascode OTA structure with class AB output buffer circuit.

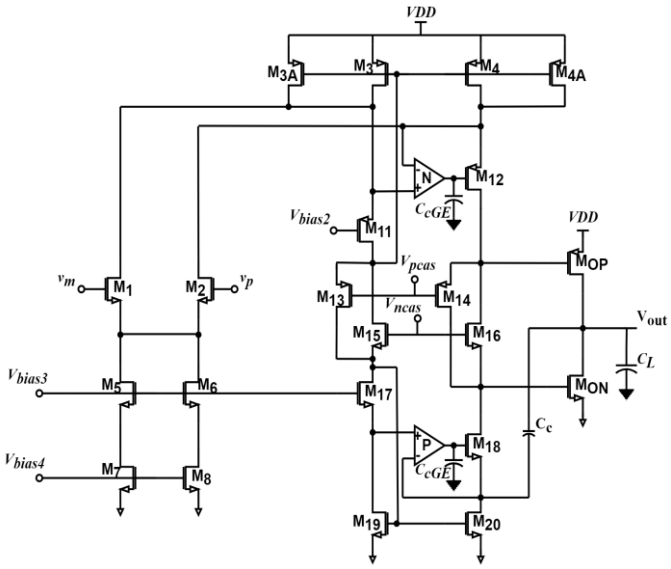

Figure 2: Proposed folded-cascode architecture

The biasing and operation of the circuits can be seen in [9]. The schematic in Figure 2 shows that the MOSFETs are in parallel in the branches that supply or sink more current. All MOSFETs in the basic folded cascode structure conduct 0.6 µA of current under equilibrium conditions. When M_1 is turned on, it pulls the drain of M_3 down, causing M_{11} to shut off. M_{17} and M_{19} pull the gate of M_3 down as M_{11} shuts down. When the gate of M_3 is closed, the current in M_4 rises. Simultaneously, as the current in M_2 decreases, the current in M_{16} increases, and the output voltage rises.

According to the equation drain current (I_D)

$$I_D = \frac{1}{2}\beta V_{ov}^2 \qquad \text{(i)}$$

Where the value of β is dependent upon the oxide capacitance and aspect ratio of the transistor.

$$\beta = \mu_n C_{ox}\left(\frac{W}{L}\right) \qquad \text{(ii)}$$

The AC drain currents of M_1 and M_2 can be written as

$$i_{d1} = -i_{d2} = g_{mn}v_{gs1} = -g_{mn}v_{gs2} \quad (1)$$

Equation 1 indicates that $v_{gs1} = -v_{gs2}$, however, we know

$$v_p - v_m = v_{gs1} + \left(-v_{gs2}\right) \qquad (2)$$

So, the drain currents (as they are equally flowing through M_1, M_3 and M_{12}), are written as

$$i_{d1} = i_{d3} = i_{d12} = \left(v_p - v_m\right)\frac{g_m}{2} \quad (3)$$

Knowing that the AC current through M_{17}/M_{19} (and thus M_{11}) is ideally zero, the current through M_{12} is then

$$i_{d12} = i_{d4} - i_{d2} = 2i_{d1} \qquad (4)$$

Hence, the output voltage is

$$v_{out} = i_{d12}\left(R_{ocasn}||R_{ocasp}\right) \qquad (5)$$

and thus, the gain is

$$A_v = \frac{v_{out}}{v_p - v_m} = g_{mn}(R_{ocasn}||R_{ocasp}) \quad \text{(A)}$$

Here gmn and gmp are the transconductance of transistors PMOS and NMOS respectively While R_{ocasn} and R_{ocasp} are the output resistance of Cascode PMOS and NMOS transistor respectively.

Proposed Folded Cascode Architecture

Figure 2 shows the schematic of the proposed folded-cascode OTA using a class AB output buffer and a gain-enhancement scheme and Figure 3 represents the diff-amps circuit configurations which serve as GE amplifiers.

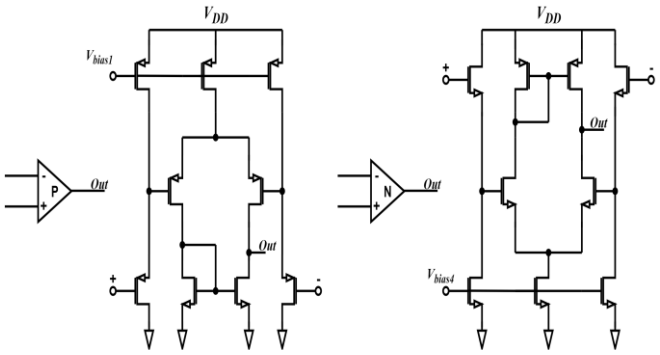

Figure 3: diff-amps

Using gain-enhancement (GE) techniques (regulating the drain node in a cascode structure), we boost the low-frequency gain by increasing the cascode output resistance. However, the gain-bandwidth product (GBW) is not affected as we get the speed by using a smaller compensation capacitor C_c and a larger diff-

amp transconductance. An additional amplifier is needed to regulate the drain of the cascode device. The source-followers on the inputs of the diff-amps as shown in Figure 3 are used to allow for the amplification of signals near ground (for the P amplifier) and V_{DD} (for the N amplifier).
The gains of the diff-amps are

$$A_P = g_{mp}(r_{on}||r_{op}), A_N = g_{mn}(r_{on}||r_{op}) \quad (B)$$

To simplify the equations, let's assume

$$A_{GE} = A_P = A_N \quad (6)$$

Hence, the low-frequency gain of the op-amp as depicted in Figure 4 is

$$A_{OLDC} = g_{mn}(R_{ocasn}||R_{ocasp}) \times (g_{mp} + g_{mn})(r_{on}||r_{op}) \quad (C)$$

So, we can write the open-loop gain with gain-enhancement as

$$A_{OLDC,GE} = A_{OLDC} \times A_{GCE} \quad (D)$$

The open-loop response of the proposed op-amp structure using the design parameters given in Table 1, is depicted in Figure 4.

Table 1: Design Parameters

Constraints/Variables	Values
W/L (PM1 - PM7)	10µm/0.1µm
W/L (PM8 - PM9)	5µm/0.1µm
W/L (NM1 - NM10)	5µm/0.1µm
W/L (NM11 - NM12)	2.5µm/0.1µm
C_{cGE}	240 fF
C_c	350 fF
C_L	100 fF

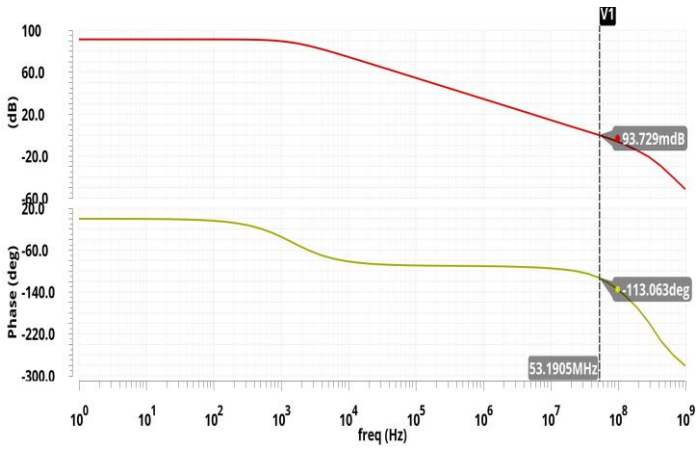

Figure 4: Frequency response of the proposed folded-cascode op-amp

The low-frequency, open-loop gain is now 91.30 dB, as shown in Figure 4. The phase margin is 66^0 and the gain-bandwidth product is increased to 3.96 MHz (by compensating the added GE amplifiers).

DC analysis of the proposed op-amp structure

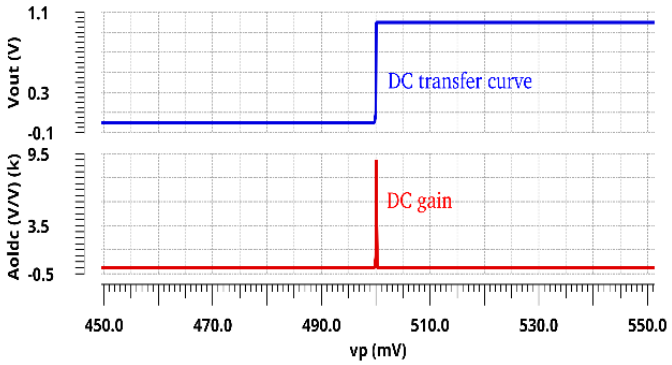

Figure 5: DC response of the proposed folded-cascode OTA with GE diff-amps.

The DC analysis has been carried out by setting $v_m = 500\ mV$ and sweeping the value of v_p over 450 mV to 550 mV. Figure 5 shows the DC transfer curve (blue curve) and open-loop DC gain (red curve) of the proposed folded-cascode OTA with class AB output buffer and GE diff-amps. The overall DC gain of the proposed op-amp is A_{OLDC} = 9450 V/V.

Step response and Slew-rate

In the transient simulation of the proposed folded-cascode OTA circuit with output buffer and GE amplifier, the bias circuit takes some time to start up, so the input signal is applied with a delay time of 100 ns. The step input signal has an amplitude of 400 mV, a period of 50 ns and a falling and rising time of 10 ps. If a larger step is applied, the small-signal analysis used to derive pole-splitting is no longer valid and as a result slew-rate limitations can be seen. Figure 6 shows the step-response of the proposed folded-cascode OTA circuit.

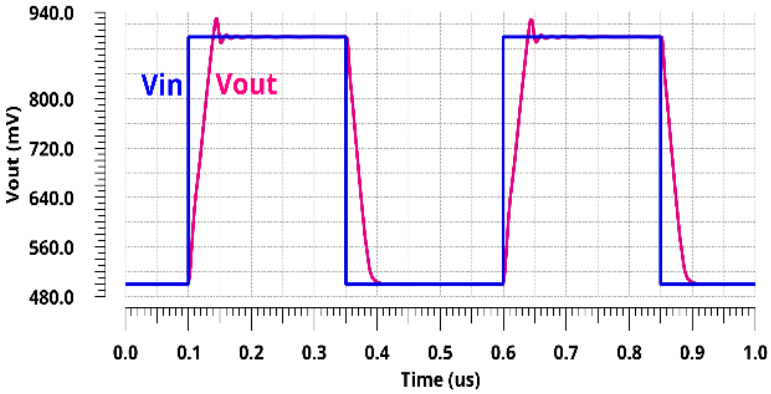

Figure 6: The large signal (500 mV to 900 mV) performance of the OTA with a good step-response. The low-to-high settling time is 50 ns, while the high-to-low settling time is 48 ns and is slew-rate limited.

The blue curve in Figure 6 depicts the step input and the purple curve shows the output step-response of the proposed folded-cascode OTA architecture. The slope of the output step-response gives the slew-rate

for the cascode OTA and is calculated as 26 V/µs. The upper spikes in the output step-response curve are due to small load capacitance i.e., C_L = 100 fF.

Noise Performance of the Proposed Architecture

Figure 7 shows how the input-referred noise sources are added to the proposed op-amp to model output noise.

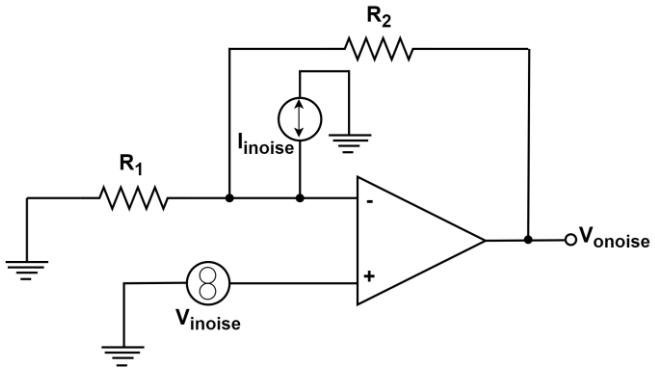

Figure 7: Modeling op-amp noise

The input-referred noise current (I_{inoise}) is connected to the inverting terminal of the op-amp, while the input-referred noise voltage (V_{inoise}) is connected in series with the non-inverting terminal.

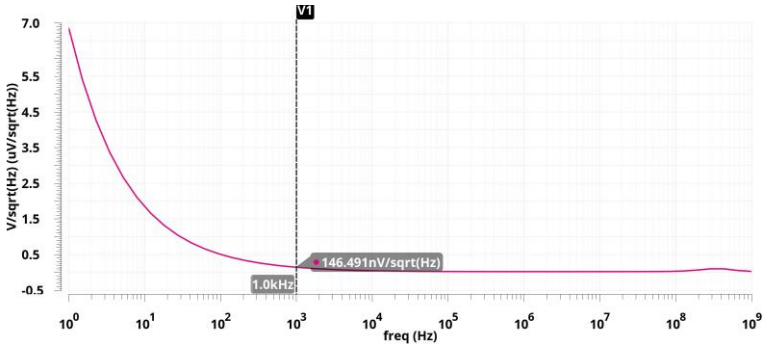

Figure 8: Input-referred noise of the proposed op-amp vs frequency

From the Figure 8, it can be seen that the input-referred noise of the proposed op-amp circuit is 146.5 nV/sqrt(Hz) at 1 kHz of input frequency.

Design specifications and performances

The design specifications and performances of the proposed cascode OTA are given in Table 2.

Table 2: OTA specifications and performances

Variables	Specifications	Performances
DC gain	> 90 dB	91.3 dB
A_{OLDC}	> 8000 V/V	9500 V/V
Phase	> 60^0	66^0
GBW	> 3 MHz	3.9 MHz
Slew-rate	> 20 V/µs	26 V/µs
Offset	2 mV to 6 mV	2.6 mV
Supply	1 V	1 V
V_{CM} (max)	980 mV	960 mV
V_{CM} (min)	450 mV	480 mV
Total current	< 150 µA	146.8 µA
Power consumed	< 150 µW	146.8 µW

2. Conclusion

We presented a design of folded-cascode OTA circuit with higher gain and bandwidth which are required in most of data converters. An output buffer class AB amplifier and two gain-enhancement diff-amps have been added to the folded-cascode amplifier to enhance the overall gain and speed of the op-amp. An industry standard 55 nm CMOS technology has been used to design the proposed folded-cascode OTA and the circuit has been simulated in CADENCE spectre. The gain and phase margins are 92.8 dB and 75^0 respectively. The proposed folded-cascode OTA structure has shown a good step-response with a slew-rate of 26 V/ns. The achieved specifications of the proposed folded-cascode OTA circuit make it suitable for data converters. This work can be extended to a three-stage folded cascode structure in order to achieve higher gain and stability.

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